

1/4

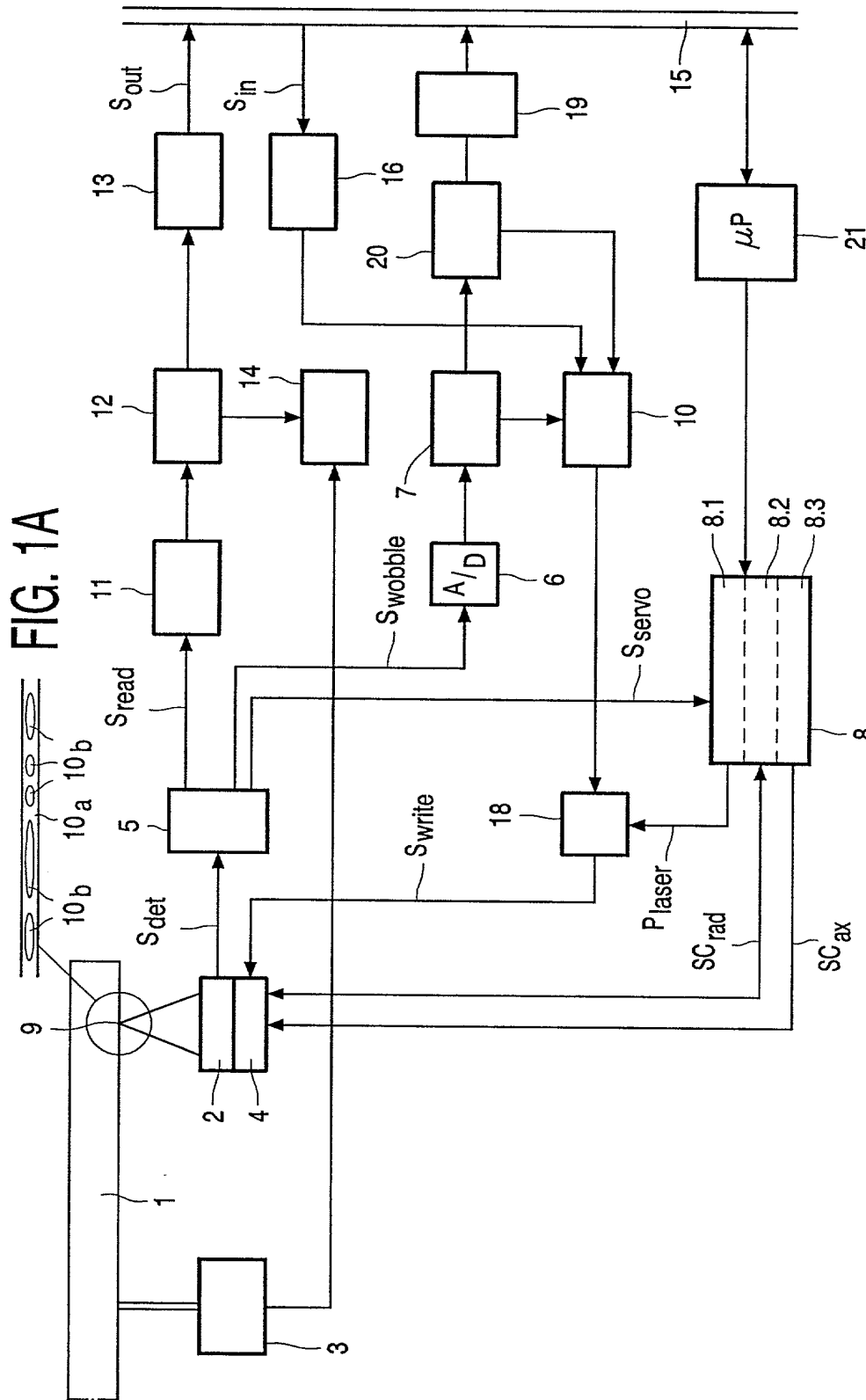


FIG. 1

FIG. 1A

The diagram shows a signal processing pipeline. It starts with an input signal S_{read} entering an A/D converter block 32. The output of block 32 is a digital signal S_{rd} . This signal is then fed into a dashed box labeled 34, which contains three sequential processing blocks: 34.1, 34.2, and 34.3. The output of block 34.3 is a signal s_{b1} . This signal s_{b1} is then fed into block 35. The final output of block 35 is b_k .

FIG 3

FIG. 3

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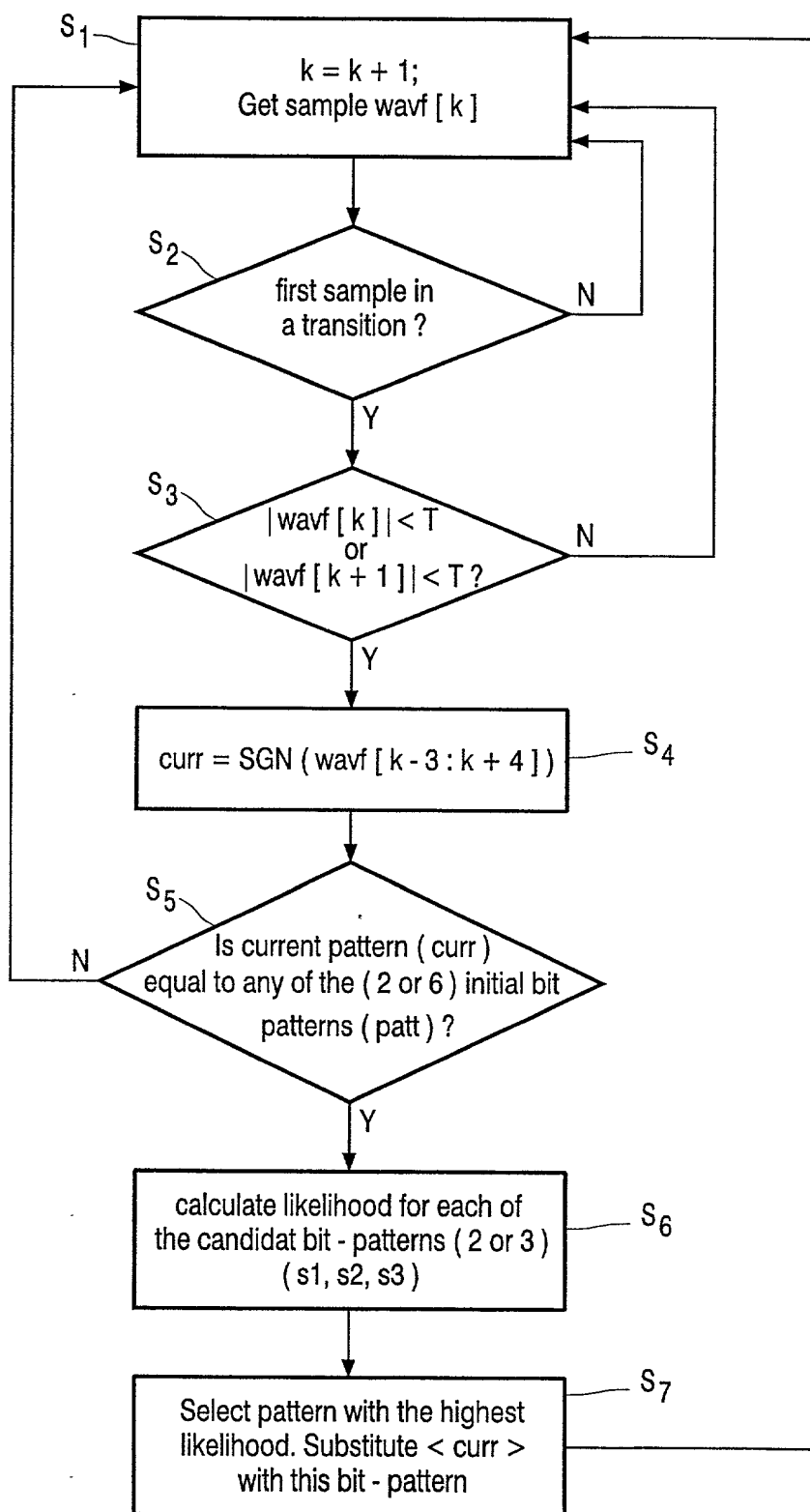


FIG. 4

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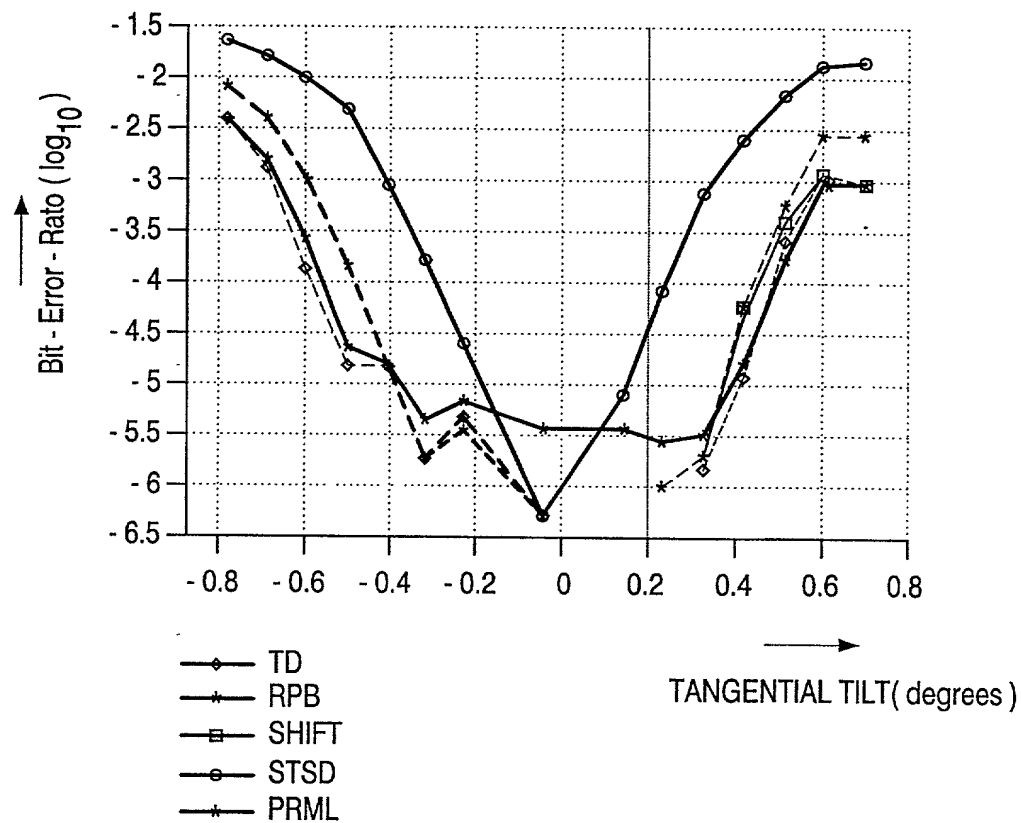


FIG. 5